

AMENDMENT TO THE CLAIMS

The following listing of claims replaces all prior versions and listings in the application:

Listing of Claims:

1. (Currently Amended) An amplifier circuit, comprising:
 - a semiconductor die;
 - a Doherty amplifier integrated on the semiconductor die, the Doherty amplifier including a peaking amplifier and a carrier amplifier coupled to the peaking amplifier;
 - a resistor divider network integrated on the semiconductor die and coupled to the carrier amplifier, the resistor divider network biasing the peaking amplifier; and
 - a self-bias circuit Field Effect Transistor integrated on the semiconductor die and coupled to the Doherty amplifier, [[; and]]
 - ~~a voltage offset circuit integrated on the semiconductor die and coupled to the bias reference circuit and to the Doherty amplifier, the voltage offset circuit the self-bias circuit Field Effect Transistor and resistor divider network together biasing the Doherty amplifier.~~
2. (Canceled)
3. (Canceled)
4. (Canceled)
5. (Currently Amended) An amplifier circuit, comprising:
 - a semiconductor die;
 - ~~at least one first and second amplifiers~~ amplifier integrated on the semiconductor die;
 - a resistor divider network integrated on the semiconductor for biasing the first amplifier;
 - and
 - a self-bias Field Effect Transistor integrated on the semiconductor die and coupled to the at least one second amplifier; and

a voltage offset circuit integrated on the semiconductor die and coupled to the bias circuit and to the at least one amplifier, the voltage offset circuit and the self-bias circuit Field Effect Transistor and resistor divider network together biasing the at least one second amplifier.

6. (Original) The amplifier circuit of claim 5, the at least one first amplifier comprising a peaking amplifier.

7. (Original) The amplifier circuit of claim 6, the at least one second amplifier comprising a carrier amplifier coupled to the peaking amplifier.

8. (Canceled)

9. (Canceled)

10. (Canceled)

11. (Currently Amended) The amplifier circuit of claim [[5]] 7, the at least one amplifier comprising a peaking amplifier being coupled to [[a]] the carrier amplifier via the resistor divider network voltage offset circuit.

12. (Currently Amended) The amplifier circuit of claim [[11]] 7, the self-bias-circuit Field Effect Transistor being coupled to the carrier amplifier.

13. (Canceled)

14. (Canceled)

15. (Currently Amended) A method, comprising:

providing a semiconductor die having an amplifier integrated on the semiconductor die, a self-bias circuit Field Effect Transistor integrated on the semiconductor die, and a voltage offset circuit resistor divider network integrated on the semiconductor die;

operating the self-bias circuit Field Effect Transistor to track device parameters of the amplifier; and

operating the self-bias circuit Field Effect Transistor and the voltage offset circuit resistor divider network to bias the amplifier based on tracked changes to the device parameters of the amplifier.

16. (Original) The method of claim 15, the amplifier comprising a peak amplifier.
17. (Original) The method of claim 15, the amplifier comprising a carrier amplifier.
18. (Canceled)
19. (Original) The method of claim 15, the step of tracking device parameters comprising tracking a threshold voltage and transconductance of the amplifier.
20. (Canceled)
21. (Canceled)
22. (Currently Amended) A method, comprising:

providing a semiconductor die having comprising

a first and second amplifier integrated on the semiconductor die;

a self-bias circuit Field Effect Transistor integrated on the semiconductor die, and

a the voltage offset circuit resistor divider network integrated on the
semiconductor die;

operating the self-bias circuit Field Effect Transistor to provide a reference voltage to the
second amplifier; and

operating the voltage offset circuit resistor divider network bias the first amplifier
proportional to the reference voltage of the second amplifier.
23. (Original) The method of claim 22, the first amplifier comprising a peaking amplifier and
the second amplifier comprising a carrier amplifier.
24. (Canceled)
25. (New) The method of claim 1, the self-bias Field Effect Transistor being coupled to a
gate terminal of the carrier amplifier.
26. (New) The method of claim 1, the self-bias Field Effect Transistor tracking device
parameters of the peaking amplifier.